

25-26-00

A

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
11675.114.1Total Pages in this Submission
23**TO THE ASSISTANT COMMISSIONER FOR PATENTS**Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

GATE STACK STRUCTURE

and invented by:

Kei-Yu KoIf a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information:☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 08/846,671

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 23 pages and including the following:
 - a. ☒ Descriptive Title of the Invention
 - b. ☒ Cross References to Related Applications (if applicable)
 - c. ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
 - d. ☐ Reference to Microfiche Appendix (if applicable)
 - e. ☒ Background of the Invention
 - f. ☒ Brief Summary of the Invention
 - g. ☒ Brief Description of the Drawings (if drawings filed)
 - h. ☒ Detailed Description
 - i. ☒ Claim(s) as Classified Below
 - j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
11675.114.1

Total Pages in this Submission
23

Application Elements (Continued)

3. ☒ Drawing(s) (when necessary as prescribed by 35 USC 113)
- a. ☒ Formal Number of Sheets 2
- b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
- a. ☐ Newly executed (original or copy) ☐ Unexecuted
- b. ☒ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional application only)
- c. ☐ With Power of Attorney ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application,
see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference (usable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under
Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby
incorporated by reference therein.
6. ☐ Computer Program in Microfiche (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all must be included)
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy (identical to computer copy)
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(B) Statement (when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
- ☐ First Class ☒ Express Mail (Specify Label No.): EL 394 376 670 US

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
11675.114.1

Total Pages in this Submission
23

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)

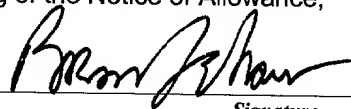
16. ☐ Additional Enclosures (please identify below):

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	20	- 20 =	0	x \$18.00	\$0.00
Indep. Claims	6	- 3 =	3	x \$78.00	\$234.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$690.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$924.00

- ☒ A check in the amount of **\$924.00** to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **23-3178** as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of _____ as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).


Signature

Bradley K. DeSandro, Reg. No. 34,521

Dated: May **25**, 2000



022901

CC:

PATENT TRADEMARK OFFICE

TRANSMITTAL LETTER
(General - Patent Pending)

Docket No.
11675.114.1

In Re Application Of: Kei-Yu Ko

1c530 U.S. PRO
09/5/9402
05/25/00

Serial No.
Not yet assigned

Filing Date
Herewith

Examiner
Not yet assigned

Group Art Unit
Not yet assigned

Title: GATE STACK STRUCTURE

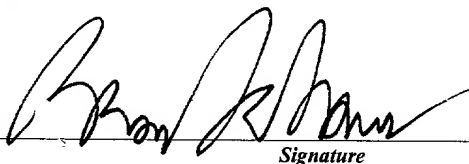
TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Utility Patent Application Transmittal (3 pgs); Divisional Application (23 pgs); Declaration and Oath; Assignment; Two (2) Sheets of Formal Drawings; Check No. 115702 in the amount of \$924.00; Certificate of Mailing by Express Mail, No. EL 394 376 670 US; Postcard

in the above identified application.

- ☐ No additional fee is required.
- ☒ A check in the amount of \$924.00 is attached.
- ☒ The Assistant Commissioner is hereby authorized to charge and credit Deposit Account No. 23-3178 as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of
- ☒ Credit any overpayment.
- ☒ Charge any additional fee required.


Signature

Dated: May 25, 2000

Bradley K. DeSandro, Reg. No. 34,521



022901

PATENT TRADEMARK OFFICE

I certify that this document and fee is being deposited on _____ with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature of Person Mailing Correspondence

Typed or Printed Name of Person Mailing Correspondence

CC:

INVENTOR INFORMATION

Inventor One Given Name:: Kei-Yu
Family Name:: Ko
Postal Address Line One:: 4611 E. Rockbury Ct.
City:: Meridian
State or Province:: Idaho
Country:: USA
Postal or Zip Code:: 83642
City of Residence:: Meridian
State or Province of Residence:: Idaho
Country of Residence:: USA
Citizenship Country:: USA

CORRESPONDENCE INFORMATION

Name Line One:: Bradley K. DeSandro
Name Line Two:: WORKMAN, NYDEGGER & SEELEY
Address Line One:: 1000 Eagle Gate Tower
Address Line Two:: 60 East South Temple
City:: Salt Lake City
State or Province:: Utah
Country:: USA
Postal or Zip Code:: 84111
Telephone One:: 801-533-9800
Fax One:: 801-328-1707
Electronic Mail One:: phuft@wnspat.com

APPLICATION INFORMATION

Title Line One:: GATE STACK STRUCTURE
Total Drawing Sheets:: 2
Formal Drawings?: Yes
Application Type:: Utility
Docket Number:: 11675.114.1
Secrecy Order in Parent Appl.?: No

REPRESENTATIVE INFORMATION

Representative Customer Number:: 22901
Registration Number One:: 34521

CONTINUITY INFORMATION

This application is a:: DIVISION OF
> Application One:: 08/846,671
Filing Date:: 04-20-1997

Source:: PrintEFS Version 1.0.1

Express Mailing Label No. EL 394 376 670 US

PATENT APPLICATION
Docket No. 11675.114.1

UNITED STATES PATENT APPLICATION

of

Kei-Yu Ko

for

GATE STACK STRUCTURE

WORKMAN, NYDEGGER & SEELEY

A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111

1 This is a divisional application of US Patent Application Serial No. 08/846,671, filed
2 on April 20, 1997, titled "UNDOPED SILICON DIOXIDE AS ETCH STOP FOR
3 SELECTIVE ETCH OF DOPED SILICON DIOXIDE", which is incorporated herein by
4 reference.

5 6 **BACKGROUND OF THE INVENTION**

7 **1. The Field of the Invention**

8 The present invention involves an etching process that utilizes an undoped silicon
9 dioxide layer as an etch stop during a selective etch of a doped silicon dioxide layer that is
10 situated on a semiconductor substrate. More particularly, the present invention relates to a
11 process for selectively utilizing a fluorinated chemistry in a plasma etch system for etching
12 a doped silicon dioxide layer situated upon an undoped silicon dioxide layer that acts as an
13 etch stop.

14 **2. The Relevant Technology**

15 Modern integrated circuits are manufactured by an elaborate process in which a large
16 number of electronic semiconductor devices are integrally formed on a semiconductor
17 substrate. In the context of this document, the term "semiconductive substrate" is defined
18 to mean any construction comprising semiconductive material, including but not limited to
19 bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies
20 comprising other materials thereon, and semiconductive material layers, either alone or in
21 assemblies comprising other materials. The term substrate refers to any supporting structure
22 including but not limited to the semiconductive substrates described above.

23 Conventional semiconductor devices which are formed on a semiconductor substrate
24 include capacitors, resistors, transistors, diodes, and the like. In advance manufacturing of
25 integrated circuits, hundreds of thousands of these semiconductor devices are formed on a
26 single semiconductor substrate. In order to compactly form the semiconductor devices, the

1 semiconductor devices are formed on varying levels of the semiconductor substrate. This
2 requires forming a semiconductor substrate with a topographical design.

3 The semiconductor industry is attempting to increase the speed at which integrated
4 circuits operate, to increase the density of devices on the integrated circuits, and to reduce
5 the price of the integrated circuits. To accomplish this task, the semiconductor devices used
6 to form the integrated circuits are continually being increased in number and decreased in
7 dimension in a process known as miniaturization.

8 One component of the integrated circuit that is becoming highly miniaturized is the
9 active region. An active region is a doped area in a semiconductor substrate that is used
10 together with other active regions to form a diode or a transistor. The miniaturization of the
11 active region complicates the formation of the interconnect structure in that, in order to
12 maintain sufficient electrical communication, the interconnect structure must be formed in
13 exact alignment with the active region. Also, the area of the interconnect structure
14 interfacing with the active region must be maximized. Thus, less area is provided as
15 tolerance for misalignment of the interconnect structure.

16 The increasing demands placed upon manufacturing requirements for the interconnect
17 structure have not been adequately met by the existing conventional technology. For
18 example, it is difficult at greater miniaturization levels to exactly align the contact hole with
19 the active region when patterning and etching the contact hole. As a result, topographical
20 structures near the bottom of the contact hole upon the active region can be penetrated and
21 damaged during etching of the contact hole. The damage reduces the performance of the
22 active region and alters the geometry thereof, causing a loss of function of the semiconductor
23 device being formed and possibly a defect condition in the entire integrated circuit. To
24 remedy these problems, the prior art uses an etch stop to prevent over etching.

25 In a conventional self-aligned etch process for a contact hole, a silicon nitride layer
26 or cap is usually used on top of a gate stack as an etch stop layer during the self-aligned

1 contact etch process. One of the problems in the prior art with forming a silicon nitride cap
2 was the simultaneous formation of a silicon nitride layer on the back side of the
3 semiconductor wafer. The particular problems depend on the process flow. For instance,
4 where a low pressure chemical vapor deposition is used to deposit silicon nitride, both sides
5 of the semiconductor wafer would receive deposits of silicon nitride. The presence of the
6 silicon nitride on the back side of the semiconductor wafer causes stress which deforms the
7 shape of the semiconductor wafer, and can also potentially cause deformation of the crystal
8 structure as well as cause defects in the circuit. Additionally, silicon nitride deposition is
9 inherently a dirty operation having particulate matter in abundance which tends to reduce
10 yield. When a low pressure chemical vapor deposition process is utilized, the silicon nitride
11 layering on the back side of the semiconductor wafer must be removed later in the process
12 flow.

1 SUMMARY OF THE INVENTION

2 The present invention relates to a process for selectively plasma etching a
3 semiconductor substrate to form a designated topographical structure thereon utilizing an
4 undoped silicon dioxide layer as an etch stop. In one embodiment, a substantially undoped
5 silicon dioxide layer is formed upon a layer of semiconductor material. A doped silicon
6 dioxide layer is then formed upon the undoped silicon dioxide layer. The doped silicon
7 dioxide layer is etched to create a topographical structure. The etch has a material removal
8 rate that is at least 10 times higher for doped silicon dioxide than for the undoped silicon
9 dioxide or the layer of semiconductor material.

10 One application of the inventive process includes a multilayer structure situated on
11 a semiconductor substrate that comprises layers of a semiconductor material, a thin silicon
12 dioxide layer, a layer of conductor material, and a refractory metal silicide layer. By way of
13 example, the multilayer structure situated on a semiconductor substrate may consist of a gate
14 oxide situated on a silicon substrate, a layer of polysilicon, and a refractory metal silicide
15 layer on the layer of polysilicon. A substantially undoped silicon dioxide layer is then
16 formed over the multilayer structure.

17 The multilayer structure is then patterned to form the designated topography. Doped
18 silicon dioxide is then formed on the semiconductor substrate as a passivation layer. A
19 photoresist layer is utilized to expose selected portions of the doped silicon dioxide layer that
20 are intended to be etched. One example of a topographical structure created utilizing this
21 process are gate stacks. The doped silicon dioxide is then selectively and anisotropically
22 etched with a carbon fluorine etch recipe so as to self-align contact holes down to the
23 semiconductor substrate between the gate stacks.

24 Each gate stack has a cap composed of substantially undoped silicon dioxide. A layer
25 of silicon nitride or undoped silicon dioxide is deposited over the gate stacks and the
26 semiconductor substrate therebetween. A spacer etch is performed to create silicon nitride

1 or undoped silicon dioxide spacers on the side of each gate stack. The silicon nitride or
2 undoped silicon dioxide spacers are generally perpendicular to the base silicon layer.

3 The present invention contemplates a plasma etching process for anisotropic etching
4 a doped silicon dioxide layer situated on an undoped silicon dioxide layer that acts as an etch
5 stop. One application of the present invention is the formation of gate stacks having spacers
6 composed of substantially undoped silicon dioxide. The undoped silicon dioxide spacers act
7 as an etch stop. Novel gate structures are also contemplated that use a substantially undoped
8 silicon dioxide etch stop layer for a carbon fluorine etch of a doped silicon dioxide layer,
9 where the substantially undoped silicon dioxide etch stop layer resists etching by a carbon
10 fluorine etch.

1

2

3

4

5

1 Figure 4 is a partial cross-sectional elevation view of the structure seen in Figure 3,
2 wherein gate stacks are formed upon the base silicon layer, each gate stack having a spacer
3 on a sidewall thereof and a cap on the top thereof, the gate stacks having deposited thereover
4 a layer of doped silicon dioxide, and a layer of photoresist is deposited upon the layer of
5 doped silicon dioxide, wherein a second selected pattern is defined in phantom which is
6 intended to represent a fluorinated chemical etch through the layer of doped silicon dioxide
7 to expose a contact on the base silicon layer that is self-aligned between the gate stacks,
8 wherein the self-alignment of the etch is due to the selectivity of the etch to the materials of
9 the spacers and the cap of the gate stacks.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The inventive process herein is directed towards selectively utilizing a plasma etch system on doped silicon dioxide (SiO₂) layer with a substantially undoped silicon dioxide layer as an etch stop. One application of the inventive process is to form a self-aligned contact. The present invention also discloses an inventive multilayer gate structure.

As illustrated in Figure 1, one embodiment of a multilayer structure 10 is created that comprises a base silicon layer 12. Overlying silicon base layer 12 is a substantially undoped silicon dioxide layer 22. Undoped silicon dioxide layer 22 can be any type of undoped oxide and be formed by a thermal process, by a plasma enhanced deposition process, or by a conventional TEOS precursor deposition that is preferably rich in carbon or hydrogen, or by a precursor of gaseous silane (SiH_4) with oxygen. In the latter process, the gaseous silane flow will result in undoped silicon dioxide layer 22.

The next layer in the embodiment of multilayer structure 10 illustrated in Figure 1 comprises a photoresist layer 24 that is processed to expose a first selected pattern 15, shown in phantom, such that silicon dioxide layer 22 will be used to create a topography in multilayer structure 10. Multilayer structure 10 is then anisotropically etched as shown by first selected pattern 15 to selectively remove material from undoped silicon dioxide layer 22 to form undoped silicon dioxide caps 16 as seen in Figure 2.

A doped silicon dioxide layer 30 is deposited over multilayer structure 10 as a passivation layer. Preferably, doped silicon dioxide layer 30 is substantially composed of borophosphosilicate glass (BPSG), borosilicate glass (BSG), or phosphosilicate glass (PSG). Most preferably, doped silicon dioxide layer 30 is substantially composed of silicon dioxide having doping of about 3% or more for boron and about 3% or more for phosphorus. A photoresist layer 32 is applied over doped silicon dioxide layer 30. Photoresist layer 32 is processed to expose a second selected portion 17 of doped silicon dioxide layer 30 that is intended to be etched. Second selected portion 17 is seen in phantom in Figure 2.

1 The structure seen in Figure 2 is now etched with a fluorinated or fluoro-carbon
 2 chemical etchant system to form second selected pattern 17 as illustrated in Figure 2. The
 3 preferred manner is an anisotropic plasma etch of doped silicon dioxide layer 30 down to the
 4 corresponding etch stop layer of undoped silicon dioxide cap 16. The plasma etch technique
 5 employed herein is preferably generated under a vacuum within the confines of a discharging
 6 unit and involves any type of a plasma system, including a high density plasma etcher. A
 7 conventional radio frequency reactive ion etcher (RF RIE) plasma system, a magnetically
 8 enhanced RIE (MERIE) plasma system, or an inductively coupled plasma system could be
 9 used. The preferred embodiment, however, is an RF type RIE or MERIE plasma system.
 10 It is preferred the plasma system being used has a plasma density in a range from about
 11 $10^9 / \text{cm}^3$ to about $10^{11} / \text{cm}^3$. A high density plasma system can also be used having a plasma
 12 density in a range from about $10^{12} / \text{cm}^3$ to about $10^{13} / \text{cm}^3$.

13 One particular embodiment of a specific structure created utilizing the inventive
 14 process is illustrated in Figure 3 wherein a multilayer structure 50 is created that comprises
 15 a base silicon layer 12. Overlying silicon base layer 12 is a gate oxide layer 14 that covers
 16 silicon base layer 12. Gate oxide layer 14 may be relatively thin in comparison with the other
 17 layers of the multilayered structure. The next layer in multilayer structure 50 comprises a
 18 polysilicon gate layer 18. Overlying polysilicon gate layer 18 is a refractory metal silicide
 19 layer 20. A known benefit of refractory metal silicides is their low resistivity. Refractory
 20 metal silicide layer 20 may comprise any refractory metal including but not limited to
 21 titanium, tungsten, tantalum, and molybdenum. Preferably, refractory metal silicide layer 20
 22 is substantially composed of tungsten silicide (WSi_x).

23 Overlying refractory metal silicide layer 20 is a substantially undoped silicon dioxide
 24 layer 22 which can be formed thermally, by plasma enhanced deposition, by a conventional
 25 TEOS precursor deposition that is preferably rich in carbon or hydrogen, or by a precursor
 26 of gaseous silane (SiH_4) with oxygen. The next layer in multilayer structure 50 is a

1 photoresist layer 24 that is processed to expose a first selected pattern 15 shown in phantom.
2 Multilayer structure 50 is then etched according to first selected pattern 15 to selectively
3 remove material so as to form gate stacks 26 as illustrated in Figure 4. Each gate stack 26
4 has an undoped silicon dioxide cap 52 thereon which was formed from undoped silicon
5 dioxide layer 22.

6 A spacer 28 in on the sidewall of each gate stack 26. Spacers 28 are formed by
7 subjecting a layer of silicon nitride deposited over gate stacks 26 to a spacer etch. Silicon
8 nitride spacers 28 are generally perpendicular to silicon base layer 12. Alternatively,
9 spacers 28 can be substantially composed of undoped silicon dioxide. As such, both
10 spacers 28 and undoped silicon dioxide caps 52 can be made from the same materials and
11 both act as an etch stop.

12 Once gate stacks 26 are formed, a contact 34 is defined therebetween upon silicon
13 base layer 12. At this point in the processing, a doped silicon dioxide layer 30, composed of
14 a material such as PSG, BSG, or BPSG, is deposited over multilayer structure 50. A
15 photoresist layer 32 is then applied over doped silicon dioxide layer 30. Photoresist layer 32
16 is processed to create a second selected pattern 17 that is illustrated in phantom in Figure 4.

17 The structure seen in Figure 4 is now etched with a fluorinated or fluoro-carbon
18 chemical etchant system according to second selected pattern 17. The preferred manner of
19 etching of doped silicon dioxide layer 30 down to its corresponding etch stop layer, which
20 is substantially undoped silicon dioxide layer 52, is by a plasma etch. The etch technique
21 employed herein is preferably a plasma etch involving any type of a plasma system including
22 a high density plasma etcher as previously discussed relative to Figure 2.

23 One factor that effects the etch rate and the etch selectivity of the process is pressure.
24 The total pressure has a preferred range from about 1 millitorr to about 400 millitorr. A more
25 preferred pressure range for a plasma etch is in a pressure range from about 1 millitorr to
26 about 100 millitorr. The most preferred pressure range for a plasma etch is from about

1 1 millitorr to about 75 millitorr. The pressure may be increased, however, above the most
2 preferred ranges. For example, the RIE etch may be performed at about 100 millitorr.
3 Selectivity can be optimized at a pressure range between about 10 millitorr and about
4 75 millitorr. Pressure increases may result in a loss in selectivity. The range in selectivity,
5 however, can be adjusted to accommodate different pressures. As such, selectivity and
6 pressure are inversely related.

7 Temperature is another factor that effects the selectivity of the etching process used.
8 A preferable temperature range during the plasma etch has a range of about 10°C to about
9 80°C, and more preferably about 20°C to about 40°C. This is the temperature of a bottom
10 electrode adjacent to silicon layer 12 during the etching process. The preferable range of the
11 semiconductor materials is between about 40°C and about 130°C, and more preferably
12 between about 40°C and about 90°C.

13 Undoped silicon dioxide cap 52 and silicon nitride spacers 28 protect gate stacks 26
14 from the fluorinated chemical etch. As illustrated in Figure 4, the etch will selectively and
15 anisotropically remove doped silicon dioxide layer 30 above contact 34 as indicated by
16 second selected pattern 17. The etch removes material from doped silicon dioxide layer 30
17 at a higher material removal rate than that of undoped silicon dioxide cap 52 and silicon
18 nitride spacers or undoped silicon dioxide spacers 28. Preferably, the etch has a material
19 removal rate for doped silicon dioxide is at least 10 times higher than that of undoped silicon
20 dioxide. As such contact 34 is self-aligned between spacers 28 of gate stacks 26. The
21 self-aligning aspect of contact 34 is due to the selectivity of the etch which assures that even
22 in cases of misalignment of the exposure of second selected pattern 17, the fluorinated
23 chemical etch through doped silicon dioxide layer 30 will properly place contact 34 on
24 silicon base layer 12 and between adjacent silicon nitride spacers 28 that have been formed
25 upon sides of gate stacks 26.

1 Contact 34 is preferably exposed by an anisotropic plasma etch with a fluorinated
2 chemistry that etches through BSG, PSG, BPSG, or doped silicon dioxide in general. The
3 etch is preferably selective to undoped silicon dioxide, silicon, and silicon nitride. The
4 fluorinated chemical etch utilizes a type of carbon fluorine gas from the group consisting of
5 C_2F_6 , CF_4 , C_3F_8 , C_4F_{10} , C_2F_8 , CH_2F_2 , CHF_3 , C_2HF_5 , CH_3F and combinations thereof. There
6 are other fluorinated enchants in a substantially gas phase during the etching of the structure.
7 An inert gas is often used in combination with the fluorinated etchant. Argon, nitrogen, and
8 helium are examples of such an inert gas. The preferred gasses, however, are CF_4 , CH_2F_2 ,
9 CHF_3 and Ar. Alternatively CH_3F may be used in place of CH_2F_2 . In particular, the
10 preferred enchant is a fluorine deficient gas which is defined as a gas where there are not
11 enough fluorine atoms to saturate the bonding for the carbon atoms.

12 A conductive material is formed upon contact 34 between spacers 28 within second
13 selected pattern 17 as shown in Figure 4. The conductive material will form a contact plug
14 to contact 34. It may be desirable to clad the contact plug with a refractory metal or a
15 refractory metal silicide. As such, second selected pattern 17 would have proximate thereto
16 the refractory metal or silicide thereof prior to formation of the contact plug in contact with
17 contact 34.

18 The present invention has application to a wide variety of structures. The top layer
19 of the gate stack, composed of undoped silicon dioxide, can be used to create and protect
20 various types of structures during the doped silicon dioxide etching process for structures
21 other than gate stacks.

22 The present invention allows the gate stack height to be reduced. One advantage of
23 reducing the gate stack height is to reduce the process time which results in greater
24 throughput. The reduced gate height results in a lower etch time and a reduced contact hole
25 aspect ratio, the latter being defined as the ratio of height to width of the contact hole. By
26 reducing the aspect ratio, or by reducing the height of the gate stack, there will be a decrease

1 in the etch time. Another advantage of a lower gate stack height is that it reduces the overall
2 topography which in turn results in it being easier to planarize and to use photolithographic
3 processes. As such, the present invention increases yield.

4 The present invention may be embodied in other specific forms without departing
5 from its spirit or essential characteristics. The described embodiments are to be considered
6 in all respects only as illustrative and not restrictive. The scope of the invention is, therefore,
7 indicated by the appended claims rather than by the foregoing description. All changes
8 which come within the meaning and range of equivalency of the claims are to be embraced
9 within their scope.

10 What is claimed and desired to be secured is:

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26

1. A gate stack structure situated over a base semiconductor material layer, said gate stack structure comprising:
 - a gate oxide layer on said base semiconductor material layer;
 - a gate layer, composed of a first conductive material, on said gate oxide layer;
 - a layer of refractory metal silicide on said gate layer;
 - an undoped silicon dioxide cap on said layer of refractory metal silicide;
 - a spacer over a lateral side of the gate layer and in contact with said base semiconductor material layer, said spacer being composed of a nonconductive material, wherein the lateral side of the gate layer is oriented perpendicular to said base semiconductor material layer;
 - a contact plug in contact with said base semiconductor material layer composed of a second conductive material, and being situated adjacent to the gate layer; and
 - a layer of doped silicon dioxide over said spacer, over said undoped silicon dioxide cap, and in contact with said contact plug.
2. The gate stack structure as recited in Claim 1, wherein said nonconductive material is composed of silicon nitride.
3. The gate stack structure as recited in Claim 1, wherein:
 - said nonconductive material is composed of undoped silicon dioxide; and
 - the spacer is integral with the undoped silicon dioxide cap.
4. The gate stack structure as recited in Claim 1, wherein the semiconductor material is monocrystalline silicon.

1 5. The gate stack structure as recited in Claim 1, wherein said refractory metal
2 silicide layer is tungsten silicide.

3
4 6. The gate stack structure as recited in Claim 1, wherein said layer of doped
5 silicon dioxide layer is composed of a material selected from the group consisting of BPSG,
6 PSG, and BSG.

7
8 7. The gate stack structure as recited in Claim 1, wherein the spacer is composed
9 of a material that is one of silicon nitride and undoped silicon dioxide.

10
11 8. The gate stack structure as defined in Claim 1, wherein the first conductive
12 material is polysilicon.

13
14

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19

9. A gate stack structure situated over a base monocrystalline silicon layer, said gate stack structure comprising:

- a gate oxide layer on said base monocrystalline silicon layer;
- a polysilicon gate layer on said gate oxide layer;
- a layer of tungsten silicide on said polysilicon gate layer;
- an undoped silicon dioxide cap on said layer of tungsten silicide;
- a spacer over a lateral side of the gate layer and in contact with said base monocrystalline silicon layer, said spacer being composed of undoped silicon dioxide and being integral with the undoped silicon dioxide cap, wherein the lateral side of the gate layer is oriented perpendicular to said base monocrystalline silicon layer;
- a contact plug in contact with said base monocrystalline silicon layer and being:
 - composed of a second conductive material; and
 - situated adjacent to the gate layer; and
 - a layer of doped silicon dioxide being composed of a material selected from the group consisting of BPSG, PSG, and BSG, and being situated over said spacer, over said undoped silicon dioxide cap, and in contact with said contact plug.

1 10. A gate stack structure situated over a base monocrystalline silicon layer, said
2 gate stack structure comprising:
3 a gate oxide layer on said base monocrystalline silicon layer;
4 a polysilicon gate layer on said gate oxide layer;
5 a layer of tungsten silicide on said polysilicon gate layer;
6 an undoped silicon dioxide cap on said layer of tungsten silicide;
7 a spacer over a lateral side of the gate layer and in contact with said base
8 monocrystalline silicon layer, said spacer being composed of of a material that is one
9 of silicon nitride and undoped silicon dioxide and being integral with the undoped
10 silicon dioxide cap, wherein the lateral side of the gate layer is oriented perpendicular
11 to said base monocrystalline silicon layer;
12 a contact plug in contact with said base monocrystalline silicon layer and
13 being:
14 composed of a second conductive material; and
15 situated adjacent to the gate layer; and
16 a layer of doped silicon dioxide being composed of a material selected from
17 the group consisting of BPSG, PSG, and BSG, and being situated over said spacer,
18 over said undoped silicon dioxide cap, and in contact with said contact plug.
19
20

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24

11. A gate structure comprising:

a pair of gate stacks situated over a base semiconductor material layer, each said gate stack comprising:

a gate oxide layer on said base semiconductor material layer;
a gate layer, composed of a first conductive material, on said gate oxide layer;

a layer of refractory metal silicide on said gate layer;
an undoped silicon dioxide cap on said layer of refractory metal silicide; and

a spacer in contact with a lateral side of each said gate stack and with said base semiconductor material layer, said spacer being composed of a nonconductive material, each said lateral side of each said gate stack being perpendicular to said base semiconductor material layer;

a contact plug in contact with said base semiconductor material layer composed of a second conductive material, and being situated between said pair of gate stacks; and

a layer of doped silicon dioxide over said spacer, over said undoped silicon dioxide cap, and in contact with said contact plug.

12. A gate structure as recited in Claim 11, wherein said nonconductive material is composed of silicon nitride.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21

13. The gate structure as recited in Claim 11, wherein:

said nonconductive material is composed of undoped silicon dioxide; and
each said spacer is integral with a respective one of said undoped silicon
dioxide caps.

14. A process as recited in Claim 11, wherein the semiconductor material is
monocrystalline silicon.

15. A process as recited in Claim 11, wherein said refractory metal silicide layer
is tungsten silicide.

16. A process as recited in Claim 11, wherein said layer of doped silicon dioxide
layer is composed of a material selected from the group consisting of BPSG, PSG, and BSG.

17. A process as recited in Claim 11, wherein the spacer is composed of a
material that is one of silicon nitride and undoped silicon dioxide.

18. A gate structure as defined in Claim 11, wherein the first conductive material
is polysilicon.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21

19. A gate structure comprising:
a pair of gate stacks situated over a base monocrystalline silicon layer, each said gate stack comprising:
a gate oxide layer on said base monocrystalline silicon layer;
a polysilicon gate layer on said gate oxide layer;
a layer of tungsten silicide on said polysilicon gate layer;
an undoped silicon dioxide cap on said layer of tungsten silicide; and
a spacer over a lateral side of each said gate stack and in contact with said base monocrystalline silicon layer, said spacer being composed of undoped silicon dioxide and being integral with the undoped silicon dioxide cap, wherein the lateral side of each said gate stack is oriented perpendicular to said base monocrystalline silicon layer;
a contact plug in contact with said base monocrystalline silicon layer and being composed of a second conductive material, and being situated between said pair of gate stacks; and
a layer of doped silicon dioxide over said spacer, over said undoped silicon dioxide cap, and in contact with said contact plug.

1 20. A gate structure comprising:

2 a pair of gate stacks situated over a base monocrystalline silicon layer, each said gate
3 stack comprising:

4 a gate oxide layer on said base monocrystalline silicon layer;

5 a polysilicon gate layer on said gate oxide layer;

6 a layer of tungsten silicide on said polysilicon gate layer;

7 an undoped silicon dioxide cap on said layer of tungsten
8 silicide; and

9 a spacer over a lateral side of each said gate stack and in
10 contact with said base monocrystalline silicon layer, said spacer being
11 composed of a material that is one of silicon nitride and undoped
12 silicon dioxide, each said lateral side of each said gate stack being
13 perpendicular to said base monocrystalline silicon layer;

14 a contact plug in contact with said base monocrystalline silicon layer and
15 being composed of a second conductive material, and being situated between said
16 pair of gate stacks; and

17 a layer of doped silicon dioxide over said spacer, over said undoped silicon
18 dioxide cap, and in contact with said contact plug.
19

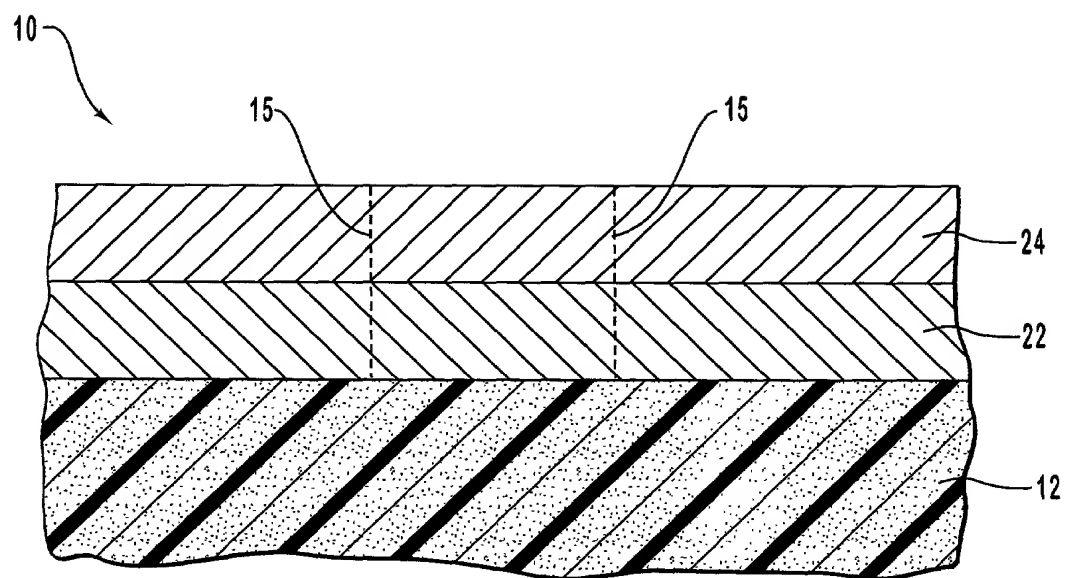


FIG. 1

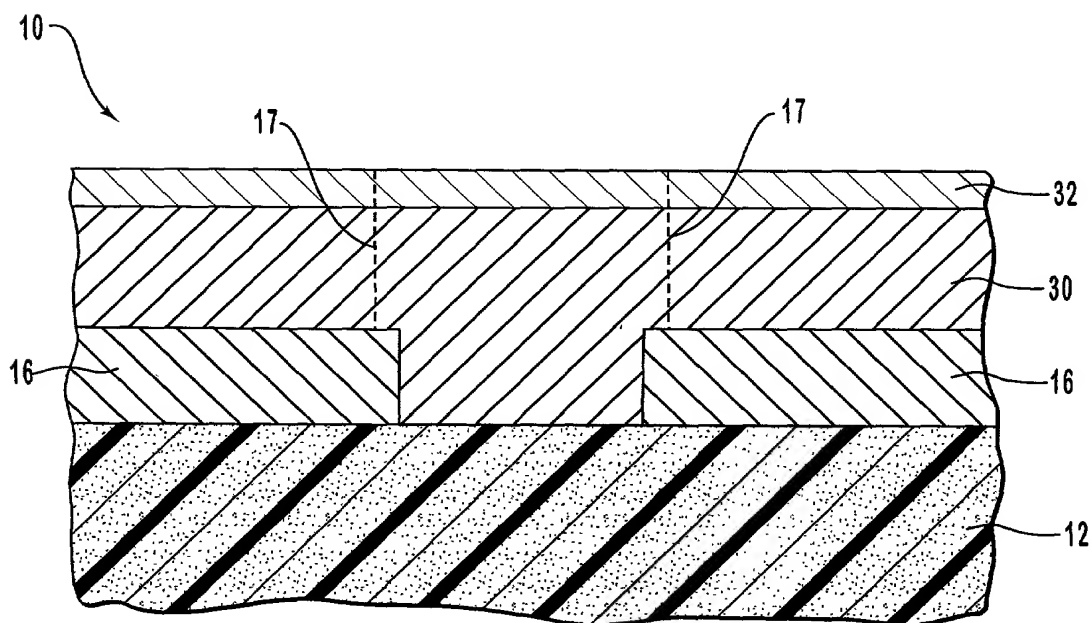
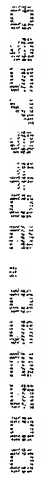
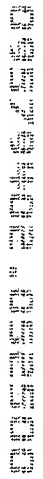


FIG. 2

[illegible]

	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2
--	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	---

DECLARATION, POWER OF ATTORNEY, AND PETITION

I, Kei-Yu Ko, declare: that I am a citizen of the United States of America; that my residence and post office address is 4611 E. Rockbury Ct., Meridian, Idaho 83642; that I verily believe I am the original, first, and sole inventor of the subject matter of the invention or discovery entitled UNDOPED SILICON DIOXIDE AS ETCH STOP FOR SELECTIVE ETCH OF DOPED SILICON DIOXIDE, for which a patent is sought and which is described and claimed in the specification attached hereto; that I have reviewed and understand the contents of the above-identified specification, including the claims; and that I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Section 1.56(a) of Title 37 of the Code of Federal Regulations.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint as my attorneys and/or patent agents: H. ROSS WORKMAN, Registration No. 25,230; RICK D. NYDEGGER, Registration No. 28,651; DAVID O. SEELEY, Registration No. 30,148; JONATHAN W. RICHARDS, Registration No. 29,843; JOHN C. STRINGHAM, Registration No. P-40,831; MICHAEL F. KRIEGER, Registration No. 35,232; BRADLEY K. DeSANDRO, Registration No. 34,521; JOHN M. GUYNN, Registration No. 36,153; GREGORY

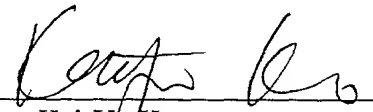
00579402 "052500"
M. TAYLOR, Registration No. 34,263; DANA L. TANGREN, Registration No. 37,246; ERIC L. MASCHOFF, Registration No. 36,596; KEVIN B. LAURENCE, Registration No. 38,219; SUSAN K. MORRIS, Registration No. 39,780, JEFFREY L. RANCK, Registration No. 38,590; C. J. VEVERKA, Registration No. P-40,858; JONATHAN D. WOOD, Registration No. 39,076; ROBYN L. PHILLIPS, Registration No. 39,330; DAVID B. DELLENBACH, Registration No. 39,166; TIMOTHY M. FARRELL, Registration No. 37,321; LENA I. VINITSKAYA, Registration No. 39,448; JOHN N. GREAVES, Registration No. 40,362, KEVIN K. JOHANSON, Registration No. 38,506; MICHAEL L. LYNCH, Registration No. 30,871; and LIA P. DENNISON, Registration No. 34,095, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith. All correspondence and telephonic communications should be directed to:

BRADLEY K. DeSANDRO
WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111

Wherefore, I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, declaration, power of attorney, and this petition.

Signed at Boise, Idaho, this 28 day of April, 1997

Inventor:


Kei-Yu Ko
4611 E. Rockbury Ct.
Meridian, Idaho 83642

G:\DATA\WPDOCS\DF\MICRON\11675114.DEC